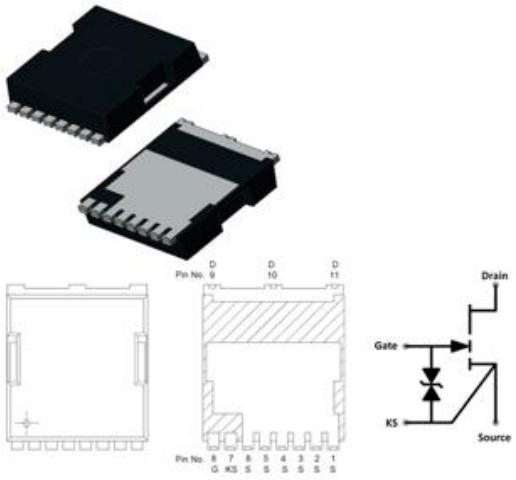
NW6503EBTL

GaN E-Mode 650V Power Transistor

Key performance parameters at Tj = 25°C		
$V_{DSS,max}$	650	V
$R_{DS(on),typ}$	28	mΩ
$Q_{G,typ}$	10.3	nC



Features

- 650V E-mode GaN FET
- TOLL 11.7x9.9 mm
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge

Applications

- AC-DC converters
- DC-DC converters
- Fast battery charging
- High density power conversion
- High efficiency power conversion

Description

The NW6503EBTL is an enhancement mode GaN transistor designed for large power density and high switching frequency. Its large threshold and gate voltage swing enable fast and safe gate driving. These features enable high efficiency and reliable power switching.

Pin Description

Pin Name	Description
1-6	Source
7	Kelvin Source
8	Gate
9-11	Drain

Absolute Maximum Ratings

T_J = 25 ˚C except as noted. Exceeding the maximum ratings may damage the device.

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source pulse Voltage	V_{DS}(pulse)	800	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source pulse Voltage	$V_{GS,pulse}$	8.5	V
Continuous drain current (T_C = 25 °C)	I_D	71.1	A
Pulsed drain current (T_C = 25 ˚C, T_{PULSE} = 1 µs)	$I_{D,pulse}$	210.5	A
Power dissipation	P_{tot}	297	W
Operating Junction Temperature	T_J	-55 to +150	˚C
Storage Temperature Range	T_S	-55 to +150	˚C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{TH,J-C,bottom}$	0.42	˚C/W
Thermal Resistance, Junction to Ambient	$R_{TH,J-A}$	45	˚C/W
Maximum reflow soldering temperature	T_{sold}	260	˚C

Electrical Characteristics

Static Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Condition
Drain-to-Source On Resistance	$R_{DS(on)}$	-	28.2	-	mΩ	I_{DS} = 18 A, V_{GS} = 6 V, T_J = 25 ˚C
		-	28	42.5	mΩ	I_{DS} = 18 A, V_{GS} = 7 V, T_J = 25 ˚C
		-	58.8	-	mΩ	I_{DS} = 18 A, V_{GS} = 7 V, T_J = 150 ˚C
Source-Drain Forward Voltage	V_{SD}	-	2.8	-	V	I_{SD} = 18 A, V_{GS} = 0 V, T_J = 25 ˚C

Gate-to-Source Threshold Voltage	$V_{GS(th)}$	0.9	1.6	2.5	V	I_{DS} = 5.2 mA, T_J = 25 ˚C
		-	1.8	-	V	I_{DS} = 5.2 mA, T_J = 150 ˚C
Gate-to-Source Forward Leakage	I_{GSS}	-	2	-	mA	V_{GS} = 7 V, V_{DS}=0V,T_J = 25 ˚C
Drain-to-Source Leakage Current	I_{DSS}	-	3	-	µA	V_{DS}=650 V, V_{GS}=0 V, T_J = 25 ˚C
		-	100	-	µA	V_{DS}=650 V, V_{GS}=0 V, T_J = 150 ˚C

Dynamic Characteristics

Input Capacitance	C_{ISS}	-	303.6	-	pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1MHz
Output Capacitance	C_{OSS}	-	118.5	-	pF	
Reverse Transfer Capacitance	C_{RSS}	-	0.85	-	pF	
6Effective Output Capacitance, Energy-Related	$C_{O(ER)}$	-	168.3	-	pF	V_{DS} = 0 V to 400 V, V_{GS} = 0 V
Effective Output Capacitance, Time-Related	$C_{O(TR)}$	-	233.9	-	pF	
Output Charge	Q_{OSS}	-	93.5	-	nC	V_{DS} = 0 V to 400 V, V_{GS} = 0 V
Gate resistance	R_G	-	1.81	-	Ω	f = 100MHz, open drain

Gate Charge Characteristics

Total Gate Charge	Q_G	-	10.3	-	nC	V_{DS} = 400 V, I_D= 18 A, V_{GS} = 0 to 7V
Gate-to-Source Charge	Q_{GS}	-	1.05	-	nC	
Gate-to-Drain Charge	Q_{GD}	-	2.85	-	nC	
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	

Reverse conduction characteristics

Pulsed current, reverse	$I_{s,\ pulse}$	-	-	210.5	A	T_C = 25 ˚C
Reverse recovery chart	Q_{rr}	-	0	-	nC	Excluding Qoss
Reverse recovery time	T_{rr}	-	0	-	nS	-
Peak reverse recovery current	I_{rrm}	-	0	-	A	-

Electrical Performance Graphs

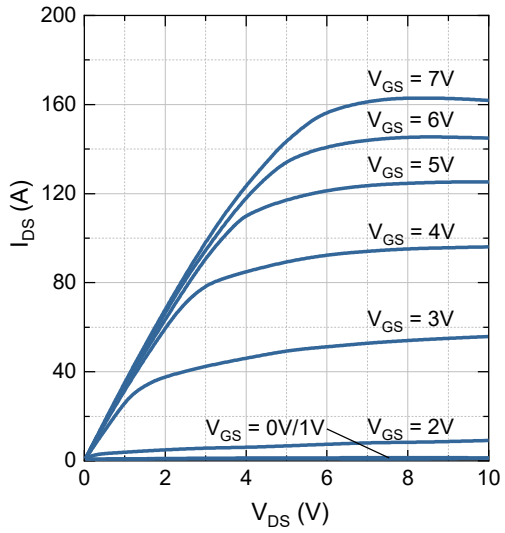


Figure 1: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 25 ˚C

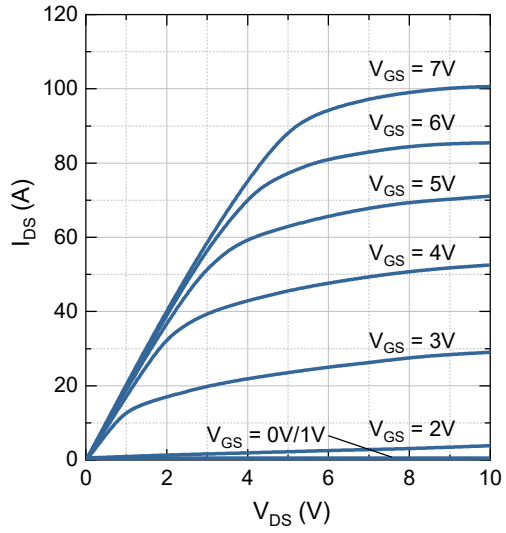


Figure 2: Typical pulsed I_{DS} vs. V_{DS} Output Characteristics at T_J = 125 ˚C

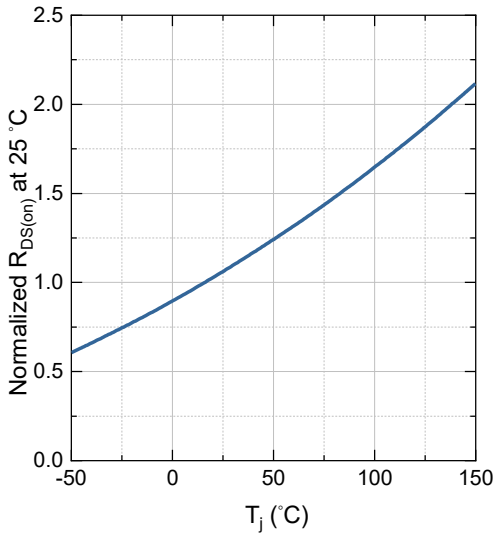


Figure 3: Normalized $R_{DS(on)}$ as a function of T_J

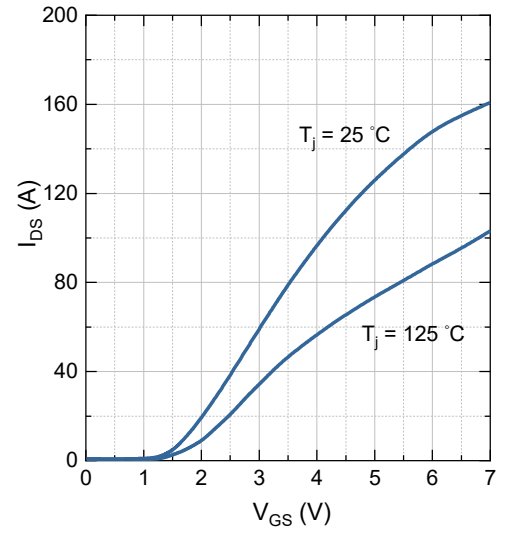


Figure 4: Typical I_{DS} vs. V_{GS} at T_J = 25 ˚C and T_J = 125 ˚C

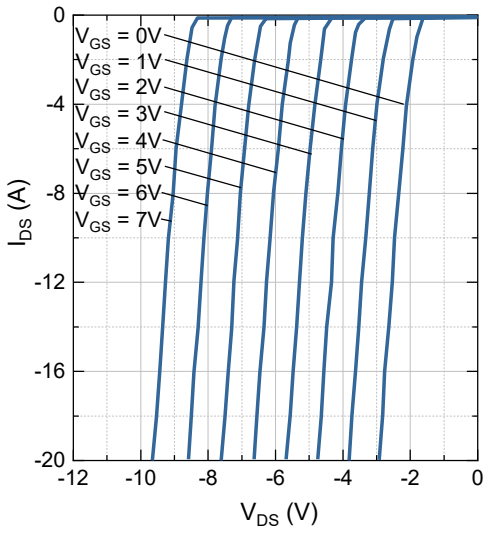


Figure 5: Typ. channel reverse characteristics (T_J =25°C)

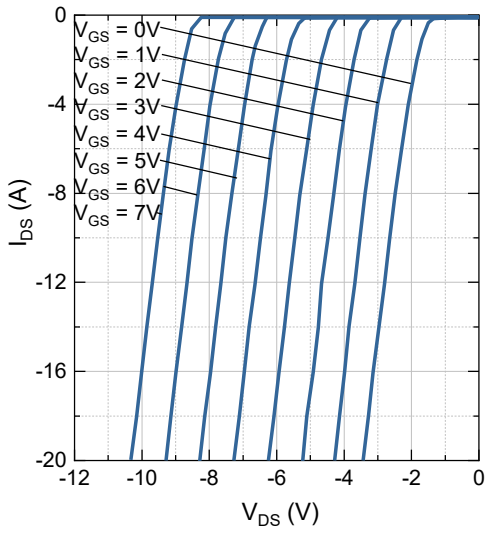


Figure 6: Typ. channel reverse characteristics (T_J =125°C)

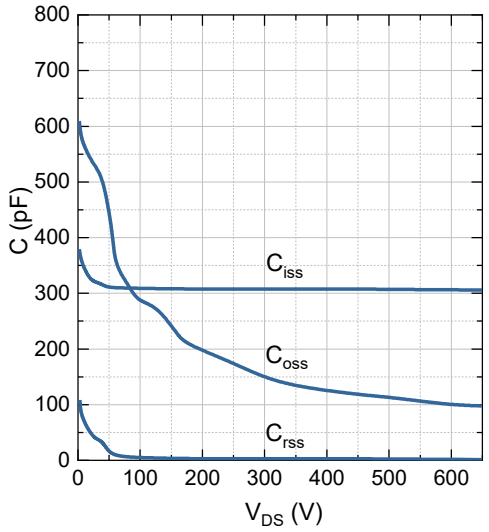


Figure 7: Typical C_{iss}, C_{oss}, C_{rss} vs. V_{DS}

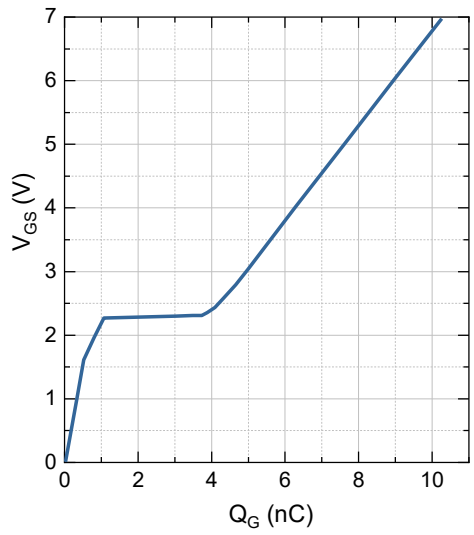


Figure 8: Typical V_{GS} vs. Q_G at V_{DS} = 400 V

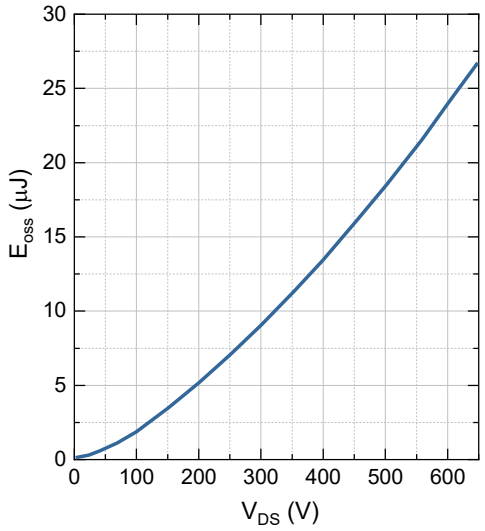


Figure 9: Typical energy stored in C_{oss}

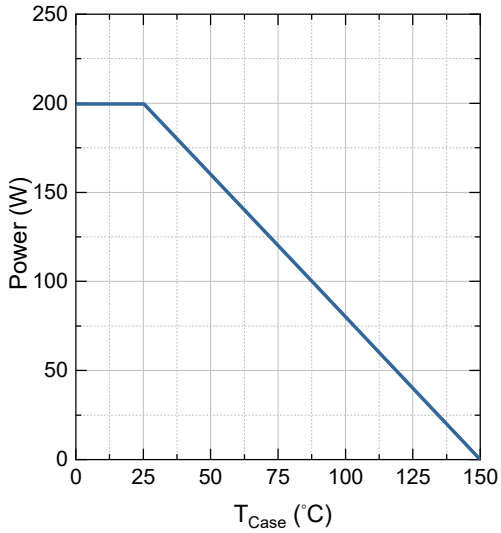


Figure 10: Power Derating vs. T_{case}

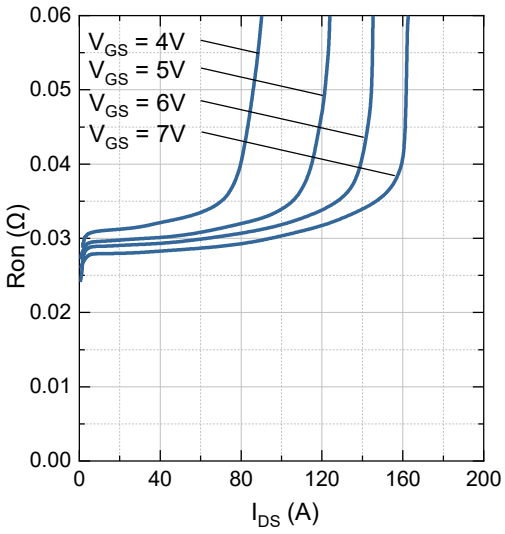


Figure 11: Typ. Drain-source on-state resistance

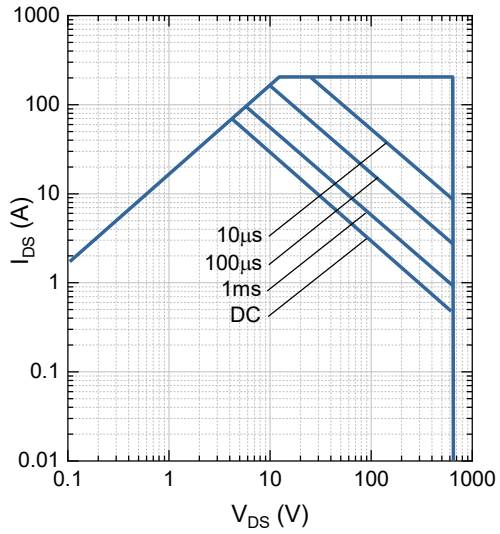


Figure 12: Safe operating area Tc=25°C

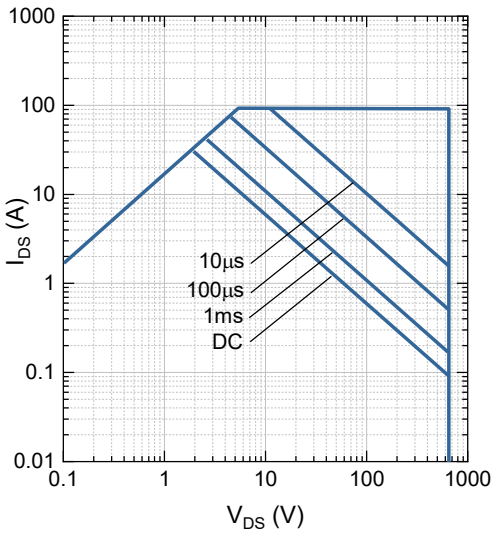


Figure 13: Safe operating area Tc=125°C

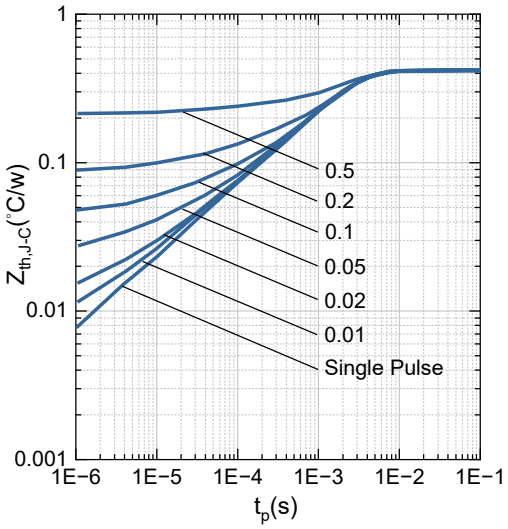
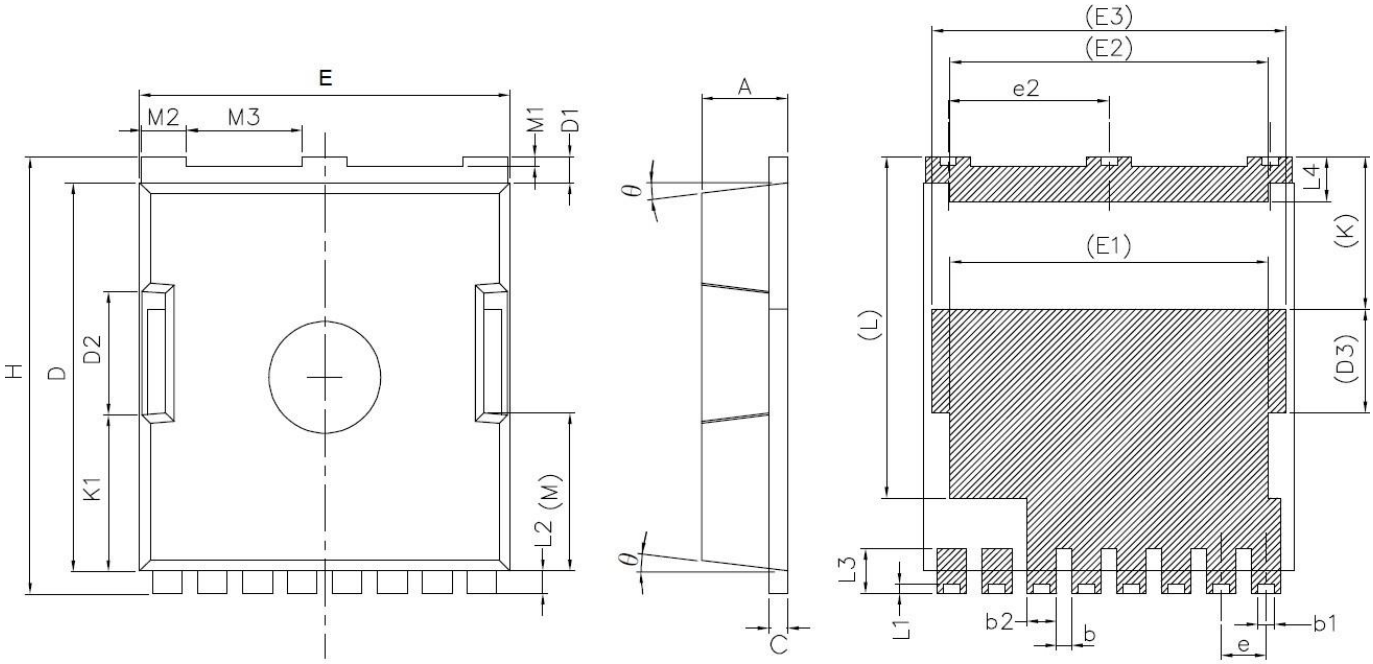
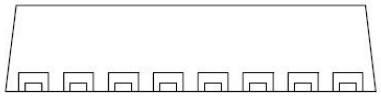


Figure 14: Max. Transient Thermal Impedance

Package Information



Side View

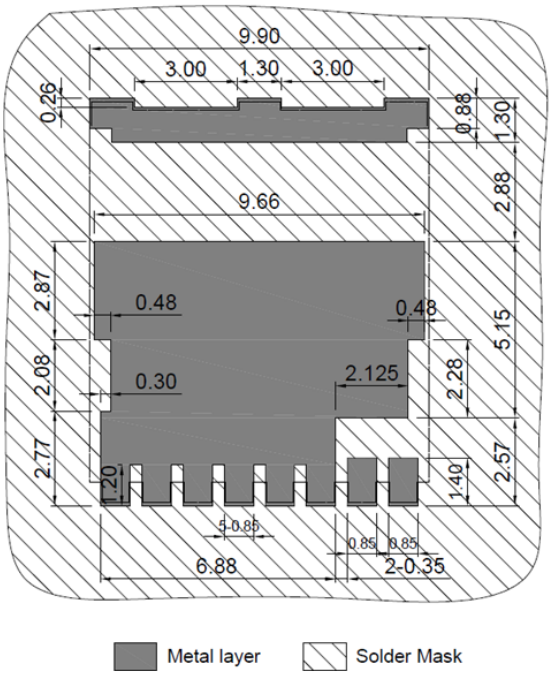


SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	2.20	2.40	H	11.48	11.88
b	0.30	0.50	K	(4.08)	
b1	0.35	0.55	K1	(4.17)	
b2	0.70	0.90	L	(9.13)	
c	0.40	0.60	L1	0.13	0.33
D	10.28	10.58	L2	0.50	0.70
D1	0.60	0.80	L3	1.10	1.30
D2	(3.30)		L4	1.10	1.30
D3	(2.77)		M	(4.23)	
E	9.70	10.10	M1	0.16	0.36
E1	(8.50)		M2	1.10	1.30
E2	(8.50)		M3	3.00	3.20
E3	(9.46)		θ	4°	10°
e	1.10	1.30	e2	4.20	4.40

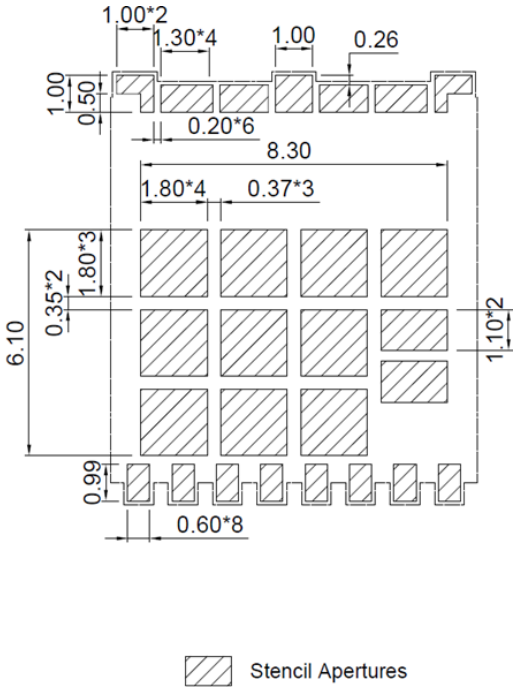
Unit : Millimeter

Recommended PCB Footprint & Stencil

Recommended PCB Footprint



Recommended Stencil apertures



All dimensions are in units mm. All pads are solder mask define. Thickness of steel plate : 100 µm

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